Implementation of RF Power MOS in 0.18μm CMOS Technology for Single Chip Solution

Heng-Ming Hsu*, Chih-Wei Chen**, Jiong-Guang Su**, Ta-Hsun Yeh**, Jason Chih-Hsien Lin**, Jack Yuan-Chen Sun**, and Chun Hsiung Chen*

*Department of Electrical Engineering, National Taiwan University, Taipei 106, Taiwan, R.O.C

**Research Development Center, Taiwan Semiconductor Manufacturing Co., Hsinchu 300, Taiwan, R.O.C

Phone: +886-3-5781688 ext.4706 Fax: +886-3-5797310 e-mail: hunming_hsu@tsmc.com.tw

Abstract - **This paper presents a complete portfolio of silicon integrated RF power MOS using 0.18μm CMOS technology in the first time. The proposed structure of power MOS promises high breakdown voltage, and presents excellent RF characteristics. To guarantee the production level, a complete qualification testing is also included.**

I. Introduction

The progress of RF CMOS technology promises the availability of communication products such as the handsets and portable applications, which have the properties of short-range transmission, low power consumption, and operated at high frequency. The previously works demonstrated the ability of single chip solution of CMOS technologies by embedding the on-chip inductors, varactors, MIM capacitors and resistors [1]. However, the power devices have not been included in the complete system on chip (SOC) solution. In addition, Silicon integrated power MOS [2-6] is inherently superior in terms of cost, compact size, and short time-to-market. Hence, the development of suitable power transistors for SOC is indispensable.

The first issue for successfully implemented power MOS is the requirement of high breakdown voltage. However, the deep-submicron technologies exhibit thinner gate oxide and shallower source/drain junction, which are a challenge for embedding power MOS. In this work, power MOS is demonstrated in a 0.18μm CMOS technology. Only one additional mask is used, and the experiment results show that the breakdown voltage of power MOS is greater than 8V. In addition, the RF performances of power MOS are also discussed. Lastly, for the consideration of mass production, the qualification of power MOS with V_t stability and gate oxide integrity is experimented to provide production level components. Based on the proposed structures, the successful implementation of power MOS is accomplished for the mass product of RF IC's.

II. DC Characteristics of Power MOS

The cross-section of power MOS is illustrated in Fig.1 (a), and the brief process flow is shown in Fig.1 (b). The additional N- implantation is used, and the N+ drain implantation offsets a distance from the edge of spacer. After source/drain formation, the oxide protect film is deposited on the offset area during silicide formation to avoid the silicidation on this area. The lower concentration of N- implantation and long offset distance of N+ at drain can reduce the electric field and impact ionization on drain side; and hence, the breakdown voltage can be enhanced. Herein, we adopt the tight spec of breakdown voltage (i.e., breakdown is started at 1nA/μm drain current). The comparison of drain junction breakdown voltage between power MOS and standard structures is shown in Fig. 2. It shows that the drain breakdown voltage can be improved approximately by 2V while adopting the proposed structure.

In addition to breakdown voltage on drain side, the snack back breakdown is also essential in power MOS design. To prevent the snack back, the reduction of impact ionization and the p-well resistance can be used. The N- side can reduce the electric field at drain side, and then reduce the impact ionization current. In addition; the source and p-well contacts can be connected together as butted contact to reduce the p-well resistance as shown in Fig. 3. Fig.4 shows the I_d-V_{ds} characteristics of butted, high substrate resistance, and standard structures. As expected, the butted structure exhibits better breakdown voltage of more than 8V. This breakdown voltage satisfies the criterion of lithium battery operation system on portable products.

III. RF Performance of Power MOS

To obtain high output power, the large total gate width of 500μm is used and arranged as finger-type in order to reduce the gate resistance as shown in Fig. 3. The p-well contacts are laid-out as guard-

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ring to prevent the substrate coupling noise, and additional p-well contacts are butted with source contacts to reduce p-well resistance. The corresponding f_T and f_{max} versus drain current I_d is shown in Fig.5. As discussed in previous section, even the offset and additional N-- implantation improve the breakdown voltage, however, the increased drain resistance also degrades the bandwidth power gain. Hence, the offset distance should be reduced to obtain an optimal distance, which satisfies the DC criterion and RF performance. As a result, power MOS with optimal offset exhibits f_T of 16GHz and f_{max} of 24GHz, resectively.

The corresponding output power at 2.4GHz can be larger than 17dBm as shown in Fig. 6. Also observed in Fig. 6, the 1dB gain compression point is 12.5 dBm, and the third-order inter-modulation point is 22.3 dBm. All the results present the high linearity of the designed power MOS. In addition, the power gain and the power-aided-efficiency (PAE) at 2.4GHz are shown in Fig. 7 with sweeping output power from −10 to 17.5 dBm, and biases at class AB. The PAE can be reach the value of 50% at output power of 16dBm, and the corresponding power gain is 12dB, which can meet the spec of Blue tooth, wireless LAN, and PHS (Personal Handy-phone System) application with the PAE, G_p, and P_{out} in this graph.

IV. Qualification Results of Power MOS

The qualification of power MOS is essential in the performance of device reliability. It involves V_t stability, and gate oxide integrity items in this study. The V_t stability using V_d=3.6V stress on 125°C after 168 hours is shown in Table 1, all the shift values on the 12 samples are within 1.29%. The gate oxide integrity is measured under V_d=6.8V, 7.0V, and 7.2V at 125°C as shown in Fig.8, using the Weibull probability model [7] to renormalize the V_d to equivalent 3.6V. It is found that the gate oxide lifetime is greater than 10^5 hours if V_d is biased at 3.6V. The result implies the fact that our power MOS can be normally operated more than 11.5 years. All the qualification items have 3 lots results and show the good reliability on power MOS devices in 0.18μm CMOS technology.

V. Conclusion

A complete portfolio of RF power MOS integrated into 0.18μm CMOS has been presented. The higher breakdown voltage of 8V has been achieved by using additional N-- implant, offset distance at drain side and the source/p-well butted connection structure. The RF performances, f_T of 16GHz, f_{max} of 24GHz, power gain of 12dB, and nearly 50% PAE with class AB bias point at 2.4GHz are addressed. To guarantee the reliability of power MOS devices, a complete qualification on V_t stability, and gate oxide integrity have been experimented. The experiment results promise the excellent capability of production of power MOS. The successful development of RF power MOS in this paper addresses the further design of short-range, low power, and high-frequency applications for integrating all components in a single chip.

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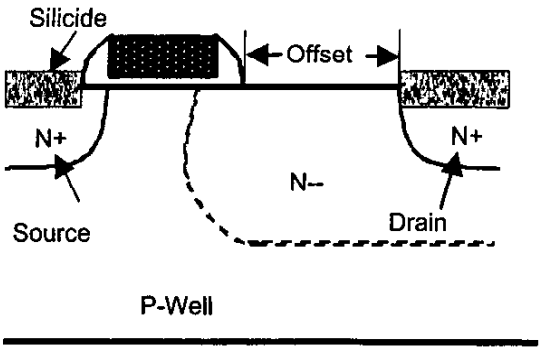

Fig.1 (a) The cross section of power MOS.

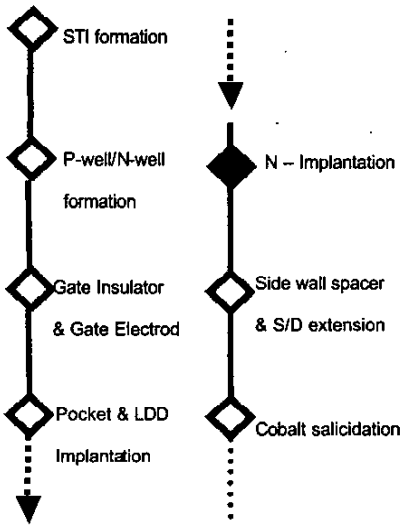

Fig.1 (b) Brief process flow of power MOS.

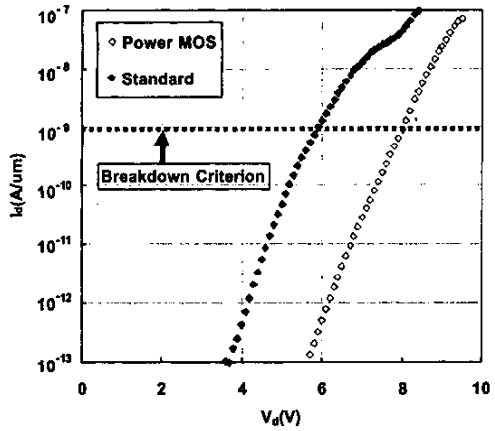

Fig.2 The junction breakdown voltage of power MOS.

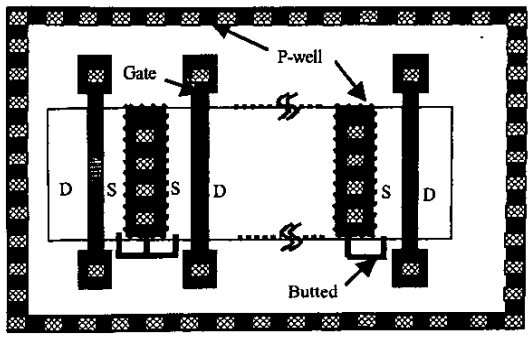

Fig.3 The top view of power MOS.

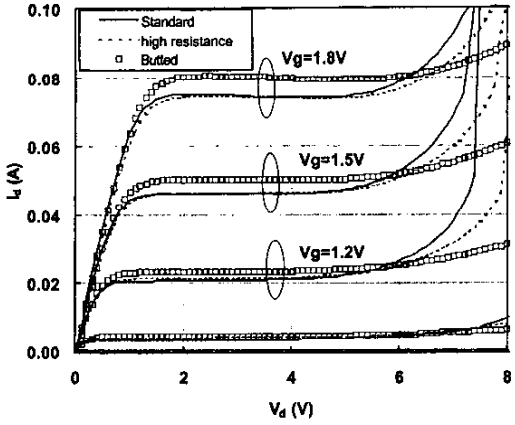

Fig.4 The I_d-V_d plots with different well pickup configurations.

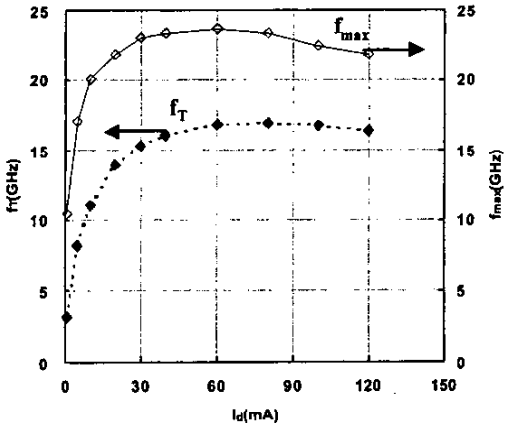

Fig.5 The plots for cutoff (f_T) and oscillation (f_{max}) frequencies.

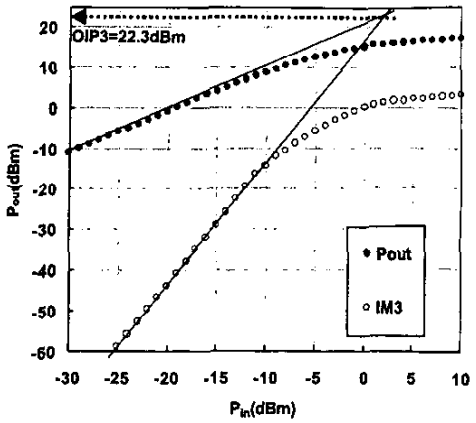

Fig.6 The plots for output and input powers.

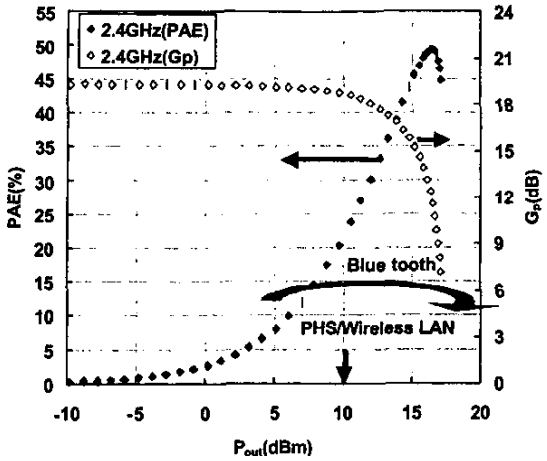

Fig.7 The plots for output power, PAE, and power gain.

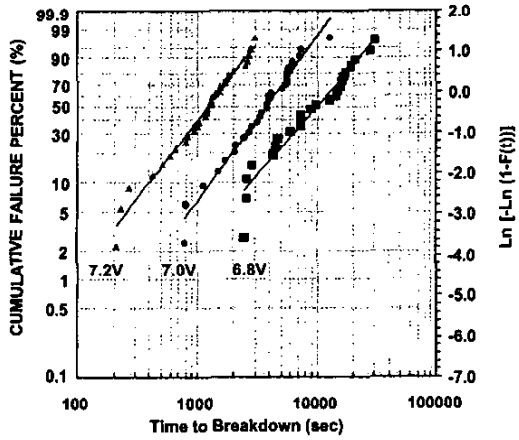

Fig.8 The oxide integrity test of power MOS.

Table.1 The V_t stability test for power MOS.

	Initial results	Burn in 168 hours results		
Die NO.	Vt	Vt	Shift (Volt.)	Shift (%)
1	0.634	0.639	0.005	0.79 %
2	0.655	0.66	0.005	0.76 %
3	0.633	0.636	0.003	0.47 %
4	0.672	0.674	0.002	0.30 %
5	0.710	0.712	0.002	0.28 %
6	0.715	0.718	0.003	0.42 %
7	0.699	0.701	0.002	0.29 %
8	0.695	0.704	0.009	1.29 %
9	0.677	0.682	0.005	0.74 %
10	0.709	0.717	0.008	1.13 %
11	0.713	0.722	0.009	1.26 %
12	0.700	0.706	0.006	0.86 %
13	0.695	0.697	0.002	0.29 %
		Max Vt Shift=	0.009	1.29 %